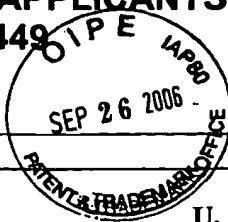


INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/29	Serial No. 09/494,567
	Applicant(s) VORBACH et al.	
	Filing Date January 31, 2000	Group Art Unit 2181



U. S. PATENT DOCUMENTS						
EXAMINER'S INITIALS	PATENT PUBLICATION NUMBER	PATENT PUBLICATION DATE	NAME	CLASS	SUB CLASS	FILING DATE*
TM A	6,697,979	February 24, 2004	Vorbach et al.			

FOREIGN PATENT DOCUMENTS							
EXAMINER'S INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION	
						YES	NO
TM B	0 726 532	August 14, 1996	EPO				

		OTHER DOCUMENTS	
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TM	1	Myers, G. "Advances in Computer Architecture," Wiley-Interscience Publication, 2nd ed., John Wiley & Sons, Inc., 1978, pp. 463-494.	
TM	2	M. Saleeba, "A Self-Contained Dynamically Reconfigurable Processor Architecture," Sixteenth Australian Computer Science Conference, ASCS-16, QLD, Australia, February, 1993, pp. 59-70.	
TM	3	Maxfield, C. "Logic that Mutates While-U-Wait" EDN (Bur. Ed) (USA), EDN (European Edition), 7 November 1996, Cahners Publishing, USA, pp. 137-140, 142.	
TM	4	Baumgarte, V., et al., PACT XPP "A Self-reconfigurable Data Processing Architecture," PACT Info. GMBH, Munchen Germany, 2001, 7 pages.	
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TM	7	Isshiki, Tsuyoshi et al., "Bit-Serial Pipeline Synthesis for Multi-FPGA Systems with C++ Design Capture," 1996 IEEE, pp. 38-47.	
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TM	9	Weinhardt, Markus et al., "Pipeline Vectorization," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 20, No. 2, February 2001, pp. 234-248.	
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TM 13	Mirsky, E. DeHon, "MATRIX: A Reconfigurable Computing Architecture with Configurable Instruction Distribution and Deployable Resources," Proceedings of the IEEE Symposium on FPGAs for Custom Computing Machines, 1996, pp. 157-166.				
TM 14	Cardoso, J.M.P., "Compilation of Java™ Algorithms onto Reconfigurable Computing Systems with Exploitation of Operation-Level Parallelism," Ph.D. Thesis, Universidade Tecnica de Lisboa (UTL), Lisbon, Portugal October 2000 (Table of Contents and <u>English Abstract only</u>).				
15	XLINX, "Logic Cell Array Families: XC4000, XC4000A and XC4000H," product description, pp. 2-7, 2-9, 2-14, 2-15, 8-16, and 9-14. NOT CONSIDERED - COPY NOT LEGIBLE				
TM 16	Hauser, J.R. et al., "Garp: A MIPS Processor with a Reconfigurable Coprocessor", University of California, Berkeley, IEEE, 1997, pages 24-33.				
TM 17	Iseli, C., et al. "A C++ Compiler for FPGA Custom Execution Units Synthesis," IEEE. 1995, pp. 173-179.				
<table border="1"> <tr> <td>EXAMINER</td> <td><i>Donald L. Memske</i></td> <td>DATE CONSIDERED</td> <td><i>10/13/2006</i></td> </tr> </table>		EXAMINER	<i>Donald L. Memske</i>	DATE CONSIDERED	<i>10/13/2006</i>
EXAMINER	<i>Donald L. Memske</i>	DATE CONSIDERED	<i>10/13/2006</i>		
<u>EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.</u>					